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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,091	03/11/2004	Richard Alan Dayan	RPS9 2003 0208 US1	6065

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,091	DAYAN ET AL.	
	Examiner	Art Unit	
	HETUL PATEL	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-10,12-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10,12-17,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the appeal brief filed on December 14, 2007.

2. Applicant's arguments have been fully considered but they are moot in view of new ground of rejection(s).

3. It appears that Applicant meant to cancel claims 11 and 18 as mentioned throughout the remarks filed on July 05, 2007, however, the status of these claims kept as "Original" instead of "Cancelled" in the Appendix of Claims in the appeal brief by mistake. Examiner considering it as claims 11 and 18 are cancelled. Therefore, claims 1-6, 8-10, 12-17 and 19-20 are currently pending in this application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 6, 8, 10, 13-15, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zwiegincew et al. (USPN: 6,633,968) in view of Brady et al. (USPN: 5,758,050).

As per claim 1, Zwiegincew teaches a method of loading data from disk in a data processing system, comprising:

- comparing a current sequence of disk requests to data indicative of a previous sequence of disk requests;

- responsive to detecting a match between the current sequence and the previous sequence, storing a copy of data blocks accessed during the current sequence in a contiguous portion of the disk (i.e. the claimed steps of comparing and detecting a match are inherent in the method taught by Zwiegincew because Zwiegincew discloses that the order in which the pages are accessed (i.e. the sequence of the disk requests) is determined based on the assumption that the disk access patterns are similar from run to run (i.e. at least one match in the sequence of disk requests is found and it is assumed that the same sequence will be called again in the next/future run); and
- responsive to a subsequent request for data in the disk sequence, mapping the request to the sequential portion of the disk and servicing the request from data in the sequential portion (e.g. see Col. 2, lines 11-24).

However, Zwiegincew failed to disclose that the contiguous portion of the disk to which the data is copied is on a different partition of the disk than a disk partition on which the original data is stored. Brady, however, teaches about storing/copying data on different partition having different operating characteristics (e.g. see Col. 2, lines 28-37). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to implement the step of prefetching and caching taught by Brady in the method taught by Zwiegincew. In doing so, it will provide flexibility in data management.

As per claim 3, the combination of Zwiegincew and Brady teaches the claimed invention as described above and furthermore, Zwiegincew teaches that storing a copy of data blocks accessed during the I/O sequence comprises storing the data blocks sequentially in the order that the data blocks were accessed chronologically (e.g. see Col. 2, lines 15-17).

As per claim 6, the combination of Zwiegincew and Brady teaches the claimed invention as described above. The further limitation of, the power-on event before the sequence of disk requests, is inherently present in the system taught by the combination of Zwiegincew and Brady because the system has to power-on before it can execute any (sequence) of disk request.

As per claims 8 and 10, see arguments with respect to rejection of claims 1 and 3, respectively. Claims 8 and 10 are also rejected based on the same rationale as the rejection of claims 1 and 3, respectively.

As per claims 14, 17 and 15, see arguments with respect to rejection of claims 1, 3 and 6, respectively. Claims 14, 17 and 15 are also rejected based on the same rationale as the rejection of claims 1, 3 and 6, respectively.

As per claims 13 and 20, the combination of Zwiegincew and Brady teaches the claimed invention as described above and furthermore, Zwiegincew teaches about updating the data in both the original data block and the copied data block in response to a modification of data in the boot sequence (e.g. see last three lines of the abstract and step 460 of Fig. 4).

5. Claims 2, 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zwiegincew in view of Brady, further in view of Hung (USPN: 5,247,653).

As per claim 2, the combination of Zwiegincew and Brady teaches the claimed invention as described above and furthermore, Zwiegincew teaches about recording disk address of each block accessed (i.e. the page reference including the physical disk sector for the page) (e.g. see Col. 3, lines 17-24). However, neither Zwiegincew nor Brady teaches about recording the length of each block. Hung, however, discloses about recording the starting address of the block and the length of the block of each memory instruction so once the controller receives the read instruction, the controller can signal the disk drive to retrieve the required number of blocks of data beginning at the starting address (e.g. see Col. 1, lines 30-44). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to implement Hung's teaching in the method taught by the combination of Zwiegincew and Brady. In doing so, the storage system performance improves since the number of times the controller must go to disk to access the data is reduced. Therefore, the data latency is reduced.

As per claims 9 and 16, see arguments with respect to rejection of claim 2. Claims 9 and 16 are also rejected based on the same rationale as the rejection of claim 2.

6. Claims 4-5, 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zwiegincew in view of Brady, further in view of Lee et al. (USPN: 2004/0260909) hereinafter, Lee.

As per claim 4, the combination of Zwiegincew and Brady teaches the claimed invention as described above. However, none of them teach about prefetching additional data and caching it in the buffer. Lee, on the other hand, teaches that upon detection of a stride, the future memory request can be predicted. The memory sequencer then prefetching the requests to read the additional data and stores/caches them into the prefetch buffer (e.g. see paragraph [0022] and Fig. 2). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to implement the step of prefetching and caching taught by Lee in the method taught by the combination of Zwiegincew and Brady. In doing so, the data will be available for processor to access from the cache instead of the disk drive. Therefore, the data latency is reduced.

As per claim 5, the combination of Zwiegincew, Brady and Lee teaches the claimed invention as described above. The further limitation of, determining whether the requested data resides in the buffer and, if so, retrieving the data from the buffering without accessing the hard disk, is inherently embedded in the system taught by Lee.

As per claims 12 and 19, see arguments with respect to rejection of claims 4 and 5. Claims 12 and 19 are also rejected based on the same rationale as the rejection of claims 4 and 5.

7. Claims 1, 3, 6, 8, 10, 13-15, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desai et al. (USPN: 6,789,171) hereinafter, Desai in view of Burr et al. (USPN: 2004/0225874) hereinafter, Burr, further in view of Delhoune et al. (USPN: 2002/0196467) hereinafter, Delhoune.

As per claim 1, Desai teaches a method of loading data from disk in a data processing system, comprising:

- comparing a current sequence of disk requests to data indicative of a previous sequence of disk requests (e.g. step 320 in Fig. 3B);
- responsive to detecting a match between the current sequence and the previous sequence, prefetching subsequent read ahead according to the stride pattern (e.g. see step 328 in Fig. 3B).

However, Desai does not teach about storing a copy of data blocks accessed during the current sequence in response to detecting a match; and mapping and servicing the subsequent request from data in the sequential portion. However, Burr teaches about storing/copying the sequence of boot data in the flash memory from the hard drive and servicing the subsequent request (i.e. subsequent booting processes) from the flash memory (e.g. see paragraphs [0029]-[0030]). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to modify the Desai's method by storing and servicing, upon detection of a match, the boot data from the flash memory instead of the hard drive as taught by Burr. In doing so, it reduces the (boot) data access time and therefore, improves the system boot-up process.

As described above, the combination of Desai and Burr discloses about storing/copying and then servicing boot data into a flash memory separate from the hard drive. Similarly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to storing/copying and then servicing boot data into a different partition of the hard drive as claimed to avoid the use of expensive flash drive.

Both Burr and Desai are silent on whether or not the sequence of boot data are stored/copied *in a contiguous portion* of the disk. Delhoune, however, discloses that a particular advantage can be obtained when (a portion of) the data are stored in the memory at *contiguous locations* such that retrieval of (the portion of) the data can be done very fast. By storing the data at *contiguous locations*, i.e. in sectors where each sector comes directly after the previous, the reading mechanism has to perform a minimum of mechanical movements (in a magnetic disk drive) so less time is consumed in reading data from disk (e.g. see paragraph [0115]). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to store/copy the boot data *in a contiguous portion* on the disk as taught by Delhoune to achieve advantages

As per claim 3, the combination of Desai, Burr and Delhoune teaches the claimed invention as described above and furthermore, Burr teaches that a signature is generated and stored in the Boot Flash to ensure that the correct boot up sequence is executed (e.g. see paragraph [0032]). Therefore, the data blocks has to be stored sequentially in the order that the data blocks were accessed chronologically otherwise

the correct boot up sequence will not be executed. Therefore, the combination of Desai, Burr and Delhoune does teach the claimed invention.

As per claim 6, the combination of Desai, Burr and Delhoune teaches the claimed invention as described above and furthermore, Burr teaches that the sequence of disk requests includes the sequence of disk requests following a power-on event (e.g. see paragraphs [0029]-[0030]).

As per claims 8 and 10, see arguments with respect to rejection of claims 1 and 3, respectively. Claims 8 and 10 are also rejected based on the same rationale as the rejection of claims 1 and 3, respectively.

As per claims 14, 17 and 15, see arguments with respect to rejection of claims 1, 3 and 6, respectively. Claims 14, 17 and 15 are also rejected based on the same rationale as the rejection of claims 1, 3 and 6, respectively.

As per claims 13 and 20, the combination of Desai, Burr and Delhoune teaches the claimed invention as described above and furthermore, Burr teaches about updating the data in both the original data block and the copied data block in response to a modification of data in the boot sequence (i.e. if the signature is not matched, then the system is booted from the hard drive and copied again in the flash memory) (e.g. paragraph [0032]).

8. Claims 4-5, 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desai in view of Burr and Delhoune, further in view of Lee.

As per claim 4, the combination of Desai, Burr and Delhoune teaches the claimed invention as described above. However, none of them teach about prefetching additional data and caching it in the buffer. Lee, on the other hand, teaches that upon detection of a stride, the future memory request can be predicted. The memory sequencer then prefetching the requests to read the additional data and stores/caches them into the prefetch buffer (e.g. see paragraph [0022] and Fig. 2). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to implement the step of prefetching and caching taught by Lee in the method taught by the combination of Desai, Burr and Delhoune. In doing so, the data will be available for processor to access from the cache instead of the disk drive. Therefore, the data latency is reduced.

As per claim 5, the combination of Desai, Burr, Delhoune and Lee teaches the claimed invention as described above. The further limitation of, determining whether the requested data resides in the buffer and, if so, retrieving the data from the buffering without accessing the hard disk, is inherently embedded in the system taught by Lee.

As per claims 12 and 19, see arguments with respect to rejection of claims 4 and 5. Claims 12 and 19 are also rejected based on the same rationale as the rejection of claims 4 and 5.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HETUL PATEL whose telephone number is (571)272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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